CLAIMS

1. A method for transmitting data on a bus with minimization of the bus switching activity, comprising the steps of:

converting the datum to be transmitted from its own original format into a transmission format that reduces the bus switching activity, said step of converting including: swapping the position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern; and selecting, between the various sorting patterns, a sorting pattern that reduces the bus switching activity upon transmission on the bus of the datum generated using said selected sorting pattern;

transmitting on the bus the datum in said transmission format; transmitting on the bus the selected sorting pattern (P_t);

receiving the datum in said transmission format; receiving the selected sorting pattern transmitted on the bus; and

converting the datum received from said transmission format to said original format using the selected sorting pattern received.

2. The method according to claim 1 wherein said step of transmitting on the bus the selected sorting pattern comprises the steps of:

generating a succession of sorting patterns identifying all the possible swaps of the position of the bit or bits of the datum to be transmitted;

comparing the optimal sorting pattern to be transmitted with the sorting patterns generated;

generating and transmitting on the bus a synchronization signal upon detection of the identity between the optimal sorting pattern to be transmitted and one of the sorting patterns generated .

3. The method according to claim 1 wherein said step of receiving the selected sorting pattern transmitted on the bus comprises the steps of:

generating a succession of sorting patterns identical to, and synchronous with, the one generated in transmission; and

identifying the sorting pattern generated at the instant of reception of the synchronization signal transmitted on the bus, the sorting pattern identified being identical to said selected sorting pattern to be transmitted.

4. The method according to claim 3 wherein the sorting pattern selected reduces the bus switching activity to a minimum amount and the sorting pattern selected is the optimal sorting pattern.

5. The method according to claim 2, characterized in that each of said steps of generating a succession of sorting patterns comprises the steps of:

providing a finite state machine having a number of internal states equal to the number of possible swaps of the position of the bit or bits of the datum to be transmitted;

associating to each of the internal states of said finite state machine a respective sorting pattern; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

6. The method according to claim 2, characterized in that each of said steps of generating a succession of sorting patterns comprises the step of:

generating a plurality of disjoint sets of sorting patterns, each set being formed by a sorting pattern identifying a respective subset of possible swaps of the position of the bit or bits of the datum to be transmitted, the sorting patterns of each set being further generated in succession and in a synchronous way with respect to the sorting patterns of the other sets.

7. The method according to claim 6, characterized in that the step of generating a plurality of separate sets of sorting patterns comprises, for each said set of sorting patterns, the steps of:

providing a finite state machine having a number of internal states equal to the number of sorting patterns in the set;

associating to each of the internal states of said finite state machine a respective sorting pattern; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding sorting patterns.

8. A device for transmitting data on a bus with minimization of the bus switching activity, comprising:

first converting means for converting the datum to be transmitted from its own original format ($b(t)$) to a transmission format ($B(t)$) that minimizes the bus switching activity, said first converter means comprising:

a swap operator for swapping the position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern (P_t); and

selecting means for selecting, between the various sorting patterns, an optimal sorting pattern (P_t) that minimizes the bus switching activity upon transmission on the bus of the datum generated using said optimal sorting pattern (P_t);

said transmission device further comprising:

transmitting means for transmitting on the bus the datum in said transmission format ($B(t)$) and the optimal sorting pattern (P_t);

receiving means for receiving the datum in said transmission format ($B(t)$) and said optimal sorting pattern (P_t) transmitted on the bus; and

second converting means for converting the datum received from said transmission format ($B(t)$) to said original format ($b(t)$) using said optimal sorting pattern (P_t) received,

said transmission device being characterized in that said transmitting means comprise:

first sorting pattern generating means for generating a succession of sorting patterns identifying all the possible swaps of the position of the bit or bits of the datum to be transmitted;

comparing means for comparing the optimal sorting pattern (P_t) to be transmitted with the sorting patterns generated;

signal generating means for generating and sending onto said bus a synchronization signal (Sync) upon detection of the identity between the optimal sorting pattern (P_t) to be transmitted and one of the sorting patterns generated,

said transmission device being further characterized in that said receiving means comprise:

second sorting pattern generating means for generating a succession of sorting patterns identical to, and synchronous with, the one generated in transmission; and

detecting means for identifying the sorting pattern generated at the instant of reception of the synchronization signal (Sync) transmitted on the bus, the sorting pattern identified being identical to said optimal sorting pattern (P_t) to be transmitted.

9. The device according to claim 8, characterized in that said first and second sorting pattern generating means each comprise a finite state machine having a number of internal states equal to the number of possible swaps of the position of the bit or bits of the datum to be transmitted, a respective sorting pattern being associated to each of the internal states of said finite state machine, said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

10. The device according to claim 8, characterized in that said first and second sorting pattern generating means each comprise a plurality of sorting pattern

modules generating a plurality of disjoint sets of sorting patterns, each set being formed by a sorting pattern identifying a respective subset of all the possible swaps of the position of the bit or bits of the datum to be transmitted, the sorting patterns of each set being further generated in succession and in a synchronous way with respect to the sorting patterns of the other sets.

11. The device according to claim 10, characterized in that each of said sorting pattern generating modules comprises a finite state machine having a number of internal states equal to the number of sorting patterns of the corresponding set, a respective sorting pattern being associated to each of the internal states of said finite state machine, said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

12. A computer product loadable into the memory of a processor associated with a bus, said computer product comprising portions of software code that can implement the method according to claim 8 when the computer product is run on a digital processor associated to the bus.

13. A method for transmitting *n*-bit data on a single line, characterized in that the transmission of a datum comprises the steps of:

generating in succession all the possible combinations of *n* bits;

comparing the *n*-bit datum to be transmitted with the combinations of *n* bits generated;

generating and transmitting on a single line an identity signal upon detection of the coincidence between the *n*-bit datum to be transmitted and one of the combinations of *n* bits generated,

and in that the reception of the datum transmitted comprises the steps of:

generating a succession of combinations of *n* bits identical to the one generated in transmission and synchronous with respect to the latter; and

identifying the combination of *n* bits generated at the instant of reception of the identity signal transmitted on the single line, the combination of *n* bits identified being identical to the *n*-bit datum to be transmitted.

14. The method according to claim 13, characterized in that said steps of generating in succession all the possible combinations of *n* bits comprises the steps of:

providing a finite state machine having a number of internal states equal to the number of possible combinations of *n* bits;

associating to each of the internal states of said finite state machine a respective combination of *n* bits; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

15. The method according to claim 13, characterized in that said steps of generating the combinations of *n* bits comprises the steps of:

generating a plurality of disjoint sets of possible combinations of *n* bits, the combinations of *n* bits of each set being further generated in succession and in a synchronous way with respect to the combinations of *n* bits of the other sets.

16. The method according to claim 15, characterized in that the step of generating a plurality of disjoint sets of possible combinations of *n* bits comprises, for each said set of combinations of *n* bits, the steps of:

providing a finite state machine having a number of internal states equal to the number of combinations of *n* bits in the set;

associating to each of the internal states of said finite state machine a respective combination of *n* bits; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

17. A device for transmitting *n*-bit data on a single line, characterized in that it comprises, at the transmission end:

first combination generating means for generating in succession all the possible combinations of *n* bits;

comparing means for comparing the *n*-bit datum to be transmitted with the combinations of *n* bits generated;

signal generating means for generating and transmitting on a single line an identity signal upon detection of the coincidence between the *n*-bit datum to be transmitted and one of the combinations of *n* bits generated;

and in that it comprises, at the reception end:

second combination generating means for generating the same succession of combinations of *n* bits generated by the first combination generating means, the successions of combinations of *n* bits generated by the said first and second combination-generating means being synchronized with one another; and

detecting means for identifying the combination of *n* bits generated at the instant of reception of the identity signal transmitted on the single line, the combination of *n* bits identified being identical to the *n*-bit datum to be transmitted.

18. The device according to claim 17, characterized in that each of said first and second combination generating means comprises a finite state machine having a number of internal states equal to the number of possible combinations of *n* bits, a respective combination of *n* bits being associated to each of the internal states of said finite state machine, and said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

19. The device according to claim 17, characterized in that said first and second combination generating means each comprise a plurality of combination generating modules generating a plurality of disjoint sets of possible combinations of *n*

bits, the combinations of *n* bits of each set being generated in succession and in a synchronous way with respect to the combinations of *n* bits of the other sets.

20. The device according to claim 19, characterized in that each of said combination generating modules comprises a finite state machine having a number of internal states equal to the number of combinations of *n* bits in the set, a respective combination of *n* bits being associated to each of the internal states of said finite state machine, and said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

21. A computer product loadable into the memory of a processor associated with a bus, said computer product comprising portions of software code that can implement the method according to claim 13 when the computer product is run on a digital processor associated to the bus.